# CSC 345 Lab – Instruction Scheduling

## *Overview*

Practice instruction scheduling. For each problem do the following:

- Show the clock cycles for the code as written without pipelining and without rearranging instructions. Show the total clock cycles.
- Show the clock cycles assuming that there is pipelining and that you can rearrange instructions. The number of clock cycles should be minimized. Show the total clock cycles.

Assume the following instruction latencies:

| **Instruction** | **Latency** |
|---|---|
| load | 3 |
| add | 1 |
| mult | 2 |
| div | 5 |

Fill out the following chart to show your answer:

| **Cycle Start** | **Cycle End** | **Instruction** |
|---|---|---|
| | | |
| | | |
| | | |
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## *Problem 1*

load r1, a
load r2, b
mult r1, r2, r3
load r4, c
load r5, d
add r4, r5, r6

## *Problem 2*

```
load r1, a
load r2, b
load r3, c
load r4, d
mult r1, r2, r5
div r3, r4, r6
```